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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,422	07/23/2004	Lars Skog	P16178-US1	8125

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EXAMINER	
MATIN, NURUL M	

ART UNIT	PAPER NUMBER
2635	

DATE MAILED: 11/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/502,422	SKOG ET AL.	
	Examiner	Art Unit	
	Nurul M. Matin	2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *11-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *11-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

VU LE
SUPERVISORY PATENT EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 375 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 11-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Doblar et al, US 6194969.

Re claim 11, Doblar discloses A computer system clocking system (fig.1, col. 3, line 4-5), said system comprising (col. 1, line 46): at least two units with clock functionality (fig. 1/#105A, 105B,col.1, line 48," master and slave (two units) phase-aligned clocks (col. 3, line 15-17), the units being coupled to a common system clock line (fig 1, col. 3, line 18-19, " the frequencies of each clock signal 106A and 106B may differ (could employ common) by an integer multiple), a common internal clock line(fig.3/#350, " local clock loads 350 could be the common internal clock line"), and a logic bus(fig. 3/ # 330,col. 5, line 34-35, " control bus 330"), wherein one unit is dedicated as a master unit at a time(col. 3, line 19-23, " if master unit fails then slave unit will take place as master unit") the dedication of the master unit being dependent on at least a signal being given so as not to select a given unit for being a master unit(col. 3, line 19-23 " master

clock signal"), and if a given unit is dedicated as master unit when such a signal is given, the system performing a switchover causing another unit as the one not selected to be dedicated as master unit(col. 3, line 23-26, col. 1, line 49-52), each unit comprising: a clock source for generating a clock source signal(col.1,line 36-38, col. 8, line 62-63), the clock source signal being adapted for being output on the internal clock line(fig.3, col.5, line 42-45); and a phase lock loop device generating a signal, which is derived from the signal on the internal clock line(fig. 3, col. 5, line 39-42) and which is output on the system clock line if the unit is dedicated as master unit(col. 5, line 40-44), wherein one source clock signal of a unit is output on the internal clock line and all phase lock loop devices of all units generate phase lock loop output signals derived from the internal clock signal, the outputs of the phase lock loop devices being in phase with one another such that switchover from one phase lock loop output signal to another is seamless.(col. 2, line 25-27, col.5. line. 65-col. 6, line 3).

Re claim 12, the system according to claim 11, wherein the unit dedicated as master unit generates the clock source signal on the internal clock line (col. 5, line 44-50)

Re claim 13, The system according to claim 11, wherein each unit further comprises: a logic section communicating with the logic bus (col. 5, line 36-38, " the control bus (logic bus) 330 provides a communications pathway between the system controller110 "); a first bidirectional port communicating with the internal clock line (; a second bidirectional port communicating with a system clock line(

col. 3, line 4-12, " it shows that the signal form clock boards 105A and 105B to system controller is a bidirectional, the logic section of the unit controlling the first and second bidirectional ports to input or output respective system clock signals and respective internal clock signals via enable signals.

Re claim 14, The system according to claim 13, wherein the enable signals first change state (106A and 106B) when the system clock is in a logic state (switching logic) with a certain predetermined security time interval from state changes of the system clock (col. 6, line 50-53, col.5, line 51-53, where clock signal for synchronization or timing means predetermined security time.

Re claim 15, the system according to claim 13, wherein the logic section, in cooperation with other logic sections of other units, negotiates a priority scheme according to which a predetermined order for dedicating units is determined (col. 6, line 54-57, " the switching logic 430 determines that the input clock 106A has failed and automatically switches over to the redundant backup clock 106B means logic section in master unit and logic section in slave unit is cooperative).

Re claim 16, The system according to claim 11, wherein the logic section of any unit comprises fault sense circuitry and wherein, if a fault is detected in any device, the system initiates switchover from a dedicated unit to a subsequent dedicated unit (col. 6, line 54-63 "the switching logic 430 determines that the input clock 106A has failed and automatically switches over to the redundant backup clock 106B").

Re claim 17, The system according to claim 11, comprising an additional board not comprising any clock generating or clock evaluating functionality, the additional board being coupled to the system clock line but not to the internal clock line nor to the logic bus (fig. 2, col. 3, line 37-39, " an embodiment of two clock boards 105A and 105B and the coupling of their respective clock signals 106A and 106B" and also system board 120).

Re claim 18, a computer system clocking unit comprising: a logic section communicating with a logic bus (as recited claim 13); a clock source for generating a clock source signal, the clock source signal being adapted for being output on an internal clock line; a phase lock loop device having a predetermined characteristic and generating a signal, which is derived from a signal on an internal clock line; first means for outputting the clock source signal to the internal clock line or inputting the internal clock signal from the internal clock line; and second means for outputting the signal from the phase lock loop device to a system clock line or inputting the system clock signal(as recited claim 11); wherein the logic section of the unit controls the first and second means to input or output respective system clock signals and respective internal clock signals(col. 6, line 3-9) and wherein, if the unit is dedicated as master unit, the logic section controls the phase lock loop generated signal derived from the internal clock signal to be output on the system clock line(col.5, line 33-38 also, col. 6, line 34-36).

Re claim 19, The computer system clocking unit according to claim 18, wherein if the unit is dedicated as master unit, the logic section controls the source clock signal to be output on the internal clock line (col. 4,line 60-65).

Re claim 20, the computer system clocking unit according to claim 18, wherein if the unit is not dedicated as master unit, the logic section controls the second means to input the system clock signal from the system clock line (col. 5, line 5-8).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Cotton et al pertains to the distributed clocking system;

b. Doblar pertains to the phase locked loop and method that provide fail-over redundant clocking;

c. Moreau pertains to the redundant clock signal generating circuitry;

d. Doblar et al pertains to the computer system including multiple clock sources and failover switching;

Contact

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nurul M. Matin whose telephone number is 571-270-1188. The examiner can normally be reached on mon-fri (7:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Le can be reached on 571-272-7332. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nurul Matin

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